

	Type	L #	Hits	Search Text	Dbs	Time Stamp	Comments	Error Definition	Errors
1	IS&R	L1	3	((("4604150") or ("5736760") or ("5913132")).PN.	USPAT; US-PGPUB	2003/05/18 14:09			0
2	BRS	L2	0	wo-0115222-\$.did.	DERWENT	2003/05/18 14:16			0
3	IS&R	L3	0	("wo-115222-\$.did.").PN.	DERWENT	2003/05/18 14:11			0
4	BRS	L4	0	wo-0115222-\$.did.	DERWENT	2003/05/18 14:17			0
5	BRS	L5	0	wo-0115222-\$.DID.	DERWENT	2003/05/18 14:12			0
6	BRS	L6	0	DE-0002650-\$.did.	DERWENT	2003/05/18 14:17			0
7	BRS	L7	0	DE-00002650-\$.did.	DERWENT	2003/05/18 14:17			0
8	BRS	L8	0	wo-00115222-\$.did.	DERWENT	2003/05/18 14:17			0
9	BRS	L9	0	wo-0115222-\$.did.	EPO; DERWENT	2003/05/18 14:16			0
10	BRS	L10	0	wo-0115222-\$.did.	EPO; DERWENT	2003/05/18 14:17			0
11	BRS	L11	0	wo-00115222-\$.did.	EPO; DERWENT	2003/05/18 14:17			0
12	BRS	L12	0	DE-0002650-\$.did.	EPO; DERWENT	2003/05/18 14:17			0
13	BRS	L13	0	DE-00002650-\$.did.	EPO; DERWENT	2003/05/18 14:26			0
14	BRS	L14	3	infineon.asn. and steck.in. and schrems.in.	EPO; DERWENT	2003/05/18 14:27			0
15	BRS	L15	0	139256.URPN.	USPAT	2003/05/18 14:30			0
16	BRS	L16	0	19956078.URPN.	USPAT	2003/05/18 14:32			0
17	BRS	FAMIL L1	1	2001-443143.NRAN.	DERWENT	2003/05/18 14:32			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Error Count
18	BRS	L18	0	20020137308.URPN.	USPAT	2003/05/18 14:33			0
19	BRS	FAMIL Y	1	2001-202948.NRAN.	DERWENT	2003/05/18 14:33			0

DERWENT-ACC-NO: 2001-202948

DERWENT-WEEK: 200329

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TITLE: Forming a trench with a buried  
trench plate comprises forming trench in substrate, forming  
non-doped silicon oxide layer and doped silicate glass  
filling, removing glass filling and non-doped silicon  
oxide layer and diffusing dopant

INVENTOR: HENNECKE, S; SCHREMS, M ; STECK, S

PATENT-ASSIGNEE: INFINEON TECHNOLOGIES AG[INFN] , SCHREMS  
M[SCHRI], STECK  
S[STECI]

PRIORITY-DATA: 1999DE-1039589 (August 20, 1999)

PATENT-FAMILY:

PUB-NO	PAGES	PUB-DATE	MAIN-IPC
TW 493269 A		July 1, 2002	N/A
000	H01L 027/108		
WO 200115222 A1		March 1, 2001	G
022	H01L 021/8242		
DE 19939589 A1		May 10, 2001	N/A
000			
US 20020137308 A1		September 26, 2002	N/A
000	H01L 027/108		
	H01L 021/76		

DESIGNATED-STATES: JP KR US AT BE CH CY DE DK ES FI FR GB  
GR IE IT LU MC NL PT  
SE

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-DESCRIPTOR	APPL-NO
TW 493269A		N/A	
2000TW-0116846		January 11, 2001	
WO 200115222A1		N/A	
2000WO-DE02650		August 3, 2000	
DE 19939589A1		N/A	
1999DE-1039589		August 20, 1999	
US20020137308A1		Cont of	
2000WO-DE02650		August 3, 2000	
US20020137308A1		N/A	
2002US-0078997		February 20, 2002	

INT-CL (IPC): H01L021/225, H01L021/76 , H01L021/762 ,  
H01L021/8242 ,  
H01L027/108

ABSTRACTED-PUB-NO: US20020137308A

#### BASIC-ABSTRACT:

NOVELTY - Process comprises forming trench (1) in substrate (2); forming non-doped silicon oxide layer (4) on trench side walls; forming a doped silicate glass filling (3); removing the glass filling and the undoped silicon oxide layer from trench upper region; and diffusing dopant from filling through undoped silicon oxide layer and forming trench plate around trench lower region in the substrate.

DETAILED DESCRIPTION - Process for forming a trench with a buried trench plate comprises forming a trench (1) having upper and lower regions in a substrate (2); forming a non-doped silicon oxide layer (4) on the trench side walls in the upper and lower regions of the trench; forming a doped silicate glass filling (3) in the upper and lower regions; removing the glass filling and the non-doped silicon oxide layer from the upper region; and diffusing the dopant from the doped filling through the undoped silicon oxide

layer and forming a trench plate in the lower region of the trench in the substrate.

USE - In the production of integrated circuits containing capacitors.

ADVANTAGE - No dopant residues remain and current leakages are avoided.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the trench structure.

Trench 1

Substrate 2

Silicate glass filling 3

Silicon oxide layer 4

ABSTRACTED-PUB-NO: WO 200115222A

EQUIVALENT-ABSTRACTS:

NOVELTY - Process comprises forming trench (1) in substrate (2); forming non-doped silicon oxide layer (4) on trench side walls; forming a doped silicate glass filling (3); removing the glass filling and the undoped silicon oxide layer from trench upper region; and diffusing dopant from filling through undoped silicon oxide layer and forming trench plate around trench lower region in the substrate.

DETAILED DESCRIPTION - Process for forming a trench with a buried trench plate comprises forming a trench (1) having upper and lower regions in a substrate (2); forming a non-doped silicon oxide layer (4) on the trench side walls in the upper and lower regions of the trench; forming a doped silicate glass filling (3) in the upper and lower regions; removing the

glass filling and the non-doped silicon oxide layer from the upper region; and diffusing the dopant from the doped filling through the undoped silicon oxide layer and forming a trench plate in the lower region of the trench in the substrate.

USE - In the production of integrated circuits containing capacitors.

ADVANTAGE - No dopant residues remain and current leakages are avoided.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the trench structure.

Trench 1

Substrate 2

Silicate glass filling 3

Silicon oxide layer 4

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: FORMING TRENCH BURY TRENCH PLATE COMPRISE  
FORMING TRENCH SUBSTRATE

FORMING NON DOPE SILICON OXIDE LAYER DOPE  
SILICATE GLASS FILL

REMOVE GLASS FILL NON DOPE SILICON OXIDE LAYER  
DIFFUSION DOPE

DERWENT-CLASS: L03 U11 U12 U13 U14

CPI-CODES: L04-C02; L04-C07E;

EPI-CODES: U11-C05G1B; U11-C07D4; U12-C02A1; U12-Q;  
U13-C04B1A; U14-A03B4;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2001-060342

Non-CPI Secondary Accession Numbers: N2001-144779

DERWENT-ACC-NO: 2001-443143

DERWENT-WEEK: 200301

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TITLE: Production of an insulating collar  
in a trench capacitor comprises forming a trench in the  
substrate, forming an insulating layer in the trench,  
filling with filler material

INVENTOR: HAUPT, M; HENNECKE, S ; KOEHLER, D ; KRASEMANN, A  
; SCHREML, M  
; KOHLER, D ; SCHREMS, M ; STECK, S

PATENT-ASSIGNEE: INFINEON TECHNOLOGIES AG[SIEI] , HAUPT  
M[HAUPI], KOHLER  
D[KOHLI], KRASEMANN A[KRASI], SCHREMS M[SCHRI],  
STECK S[STECI]

PRIORITY-DATA: 1999DE-1056078 (November 22, 1999)

PATENT-FAMILY:

PUB-NO	PAGES	PUB-DATE	MAIN-IPC
US 20020182819 A1		December 5, 2002	N/A
000	H01L 021/20		
DE 19956078 A1		May 31, 2001	N/A
011	H01L 021/8242		
WO 200139256 A2		May 31, 2001	G
000			
	H01L 021/00		

DESIGNATED-STATES: US AT BE CH CY DE DK ES FI FR GB GR IE  
IT LU MC NL PT SE TR

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-DESCRIPTOR	APPL-NO
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US20020182819A1	Cont of
2000WO-DE04114	November 22, 2000
US20020182819A1	N/A
2002US-0153045	May 22, 2002
DE 19956078A1	N/A
1999DE-1056078	November 22, 1999
WO 200139256A2	N/A
2000WO-DE04114	November 22, 2000

INT-CL (IPC): H01L021/00, H01L021/20 , H01L021/8242

ABSTRACTED-PUB-NO: DE 19956078A

BASIC-ABSTRACT:

NOVELTY - Production of an insulating collar in a trench capacitor comprises:

- (a) preparing a semiconductor substrate (5), forming a trench (10) in the substrate;
- (b) forming an insulating layer (35) in the trench to form an insulating collar (75);
- (c) filling a lower region (50) of the trench with a sacrificial filler material (40) so that an upper region (45) of the trench remains free from the filler material;
- (d) forming a structured layer on the insulating layer and on the filler material;
- (e) forming an opening (60) in the structured layer, removing the filler material; and
- (f) removing the insulating layer from the lower region by etching the insulating layer selectively to the structured layer.

DETAILED DESCRIPTION - Preferred Features: The structured layer and the filler

material are made of silicon nitride, polysilicon,  
amorphous silicon or  
photolacquer.

USE - Used in RAMs

ADVANTAGE - The collar is reliable.

DESCRIPTION OF DRAWING(S) - The drawing shows a section  
through the capacitor.

Substrate 5

Trench 10

Insulating layer 35

Filler material 40

Upper region 45

Lower region 50

Opening 60

CHOSEN-DRAWING: Dwg.1B/2

TITLE-TERMS: PRODUCE INSULATE COLLAR TRENCH CAPACITOR  
COMPRISE FORMING TRENCH  
SUBSTRATE FORMING INSULATE LAYER TRENCH FILL  
FILL MATERIAL

DERWENT-CLASS: L03 U11 U12 U13 U14

CPI-CODES: L03-G04A; L04-C12C; L04-C14A;

EPI-CODES: U11-C05B5; U11-C05G1B; U11-C07D4; U11-C08A3;  
U12-C02A1; U12-Q;  
U13-C04B1A; U14-A03B4;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2001-134190

Non-CPI Secondary Accession Numbers: N2001-327779